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Jpn. J. Appl. Phys. **49** (2010) 04DC13

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Japanese Journal of Applied Physics **49** (2010) 04DC13 **REGULAR PAPER**

New Source Heterojunction Structures with Relaxed/Strained Semiconductors for Quasi-Ballistic Complementary Metal–Oxide–Semiconductor Transistors: Relaxation Technique of Strained Substrates and Design of Sub-10 nm Devices

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Received October 2, 2009; revised November 10, 2009; accepted November 10, 2009; published online April 20, 2010

We have studied new abrupt-source-relaxed/strained semiconductor-heterojunction structures for quasi-ballistic complementary metal–oxide–semiconductor (CMOS) devices, by locally controlling the strain of a single strained semiconductor. Appling O^+ ion implantation recoil energy to the strained semiconductor/buried oxide interface, Raman analysis of the strained layers indicates that we have successfully relaxed both strained-Si-on-insulator (SSOI) substrates for n-MOS and SiGe-on-insulator (SGOI) substrates for p-MOS without polycrystallizing the semiconductor layers, by optimizing O^+ ion implantation conditions. As a result, it is considered that the source conduction and valence band offsets ΔE_C and ΔE_V can be realized by the energy difference in the source Si/channel-strained Si and the source-relaxed SiGe/channel-strained SiGe layers, respectively. The device simulator, considering the tunneling effects at the source heterojunction, shows that the transconductance of sub-10 nm source heterojunction MOS transistors (SHOT) continues to increase with increasing ΔE_C. Therefore, SHOT structures with the novel source heterojunction are very promising for future quasi-ballistic CMOS devices.
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DOI: 10.1143/JJAP.49.04DC13

1. Introduction

Device performance saturation in a scaled complementary metal–oxide–semiconductor (CMOS) has been a serious problem in realizing high performance ultralarge scale integrations (ULSIs).[1)] Utilization of quasi-[2)] and ballistic carrier transports[3–5)] in ultrascaled MOS field-effect transistors (MOSFETs) is a key technology for future high-speed CMOS circuits. However, the injected carrier velocity at the source edge is limited by thermal velocity or Fermi velocity.[3–5)] In order to overcome the above physical limitation, several MOSFET structures realized by source engineering, such as hot-electron transistors[6)] and source-Schottky barrier structures,[7)] have been proposed. In particular, in a heterojunction bipolar transistor (HBT),[8,9)] a wide-gap emitter can inject higher-velocity carriers into a narrow-gap base region, using excess kinetic energy due to the band offset at the emitter/base heterojunction. Therefore, an application of the concept of high-velocity carrier injection in HBT technology to the source/channel edge in MOSFETs can provide a solution to the above-mentioned physical limitation on carrier velocity in conventional MOSFET structures, leading to the realization of ballistic MOSFETs. We have experimentally demonstrated high-performance source heterojunction MOS transistors (SHOTs) for quasi-ballistic electron transport. Using an excess kinetic energy corresponding to the conduction band offset ΔE_C at the source-relaxed SiGe/channel-strained Si heterojunction edge, we have demonstrated high-velocity electron injection into the channel from source regions.[10,11)] However, the SiGe/strained Si heterostructures can be used only for n-MOS, because there is no valence band offset in the SiGe/strained Si heterostructures. Therefore, another source heterostructure is required to realize p-channel SHOTs. Moreover, the Ge atom diffusion into the channel from the source SiGe layer leads to a graded heterojunction, resulting in the reduction of injected electron velocity in the SHOTs.[12)] In order to overcome the above-mentioned problems, new source heterojunction structures for CMOS-SHOTs based on a single semiconductor are strongly required.[12)]

In this work, we have experimentally studied a new abrupt source-heterojunction structure with lateral relaxed/strained semiconductor layers consisting of a single semiconductor.[13)] Namely, these new source heterojunctions can be easily formed by local O^+ ion implantation-induced relaxation effects of strained substrates. Moreover, the source conduction and the valence band offsets for n- and p-MOSs can be realized by lateral source-relaxed Si/channel Si with a tensile strain and source-relaxed SiGe/channel SiGe with a compressive strain, respectively. By O^+ ion implantation into a strained-Si-on-insulator (SSOI) substrate for n-MOS and a SiGe-on-insulator (SGOI) substrate for p-MOS, we have successfully relaxed both SSOI and SGOI substrates without polycrystallizing the strained substrates. The relaxation mechanism for both SSOIs and SGOIs has been explained by the recoil energy of O^+ ions at the strained-semiconductor/buried-oxide interface.

2. Concept for Novel Source Heterojunction CMOS Structures and Experiment

Figure 1 shows a schematic n-channel SHOT structures fabricated by a conventional source relaxed-SiGe/strained Si heterojunction. An ideal velocity increase Δv of the injected electrons in SHOTs can be expressed by $\Delta v = (2\Delta E_C/m_T^*)^{1/2}$, where m_T^* is the transverse effective mass of inversion electrons of the channel. Therefore, a higher ΔE_C and a lower m_T^* are required to increase Δv in SHOTs. Moreover, Figs. 2(a) and 2(b) show E_C profiles of abrupt and linear graded source heterojunctions, respectively. In the case of the abrupt source heterojunction, electrons from the source region can obtain a kinetic energy from the

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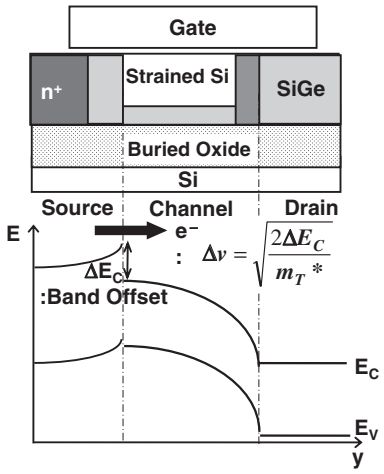

Fig. 1. Schematic of n-channel SHOT structures fabricated using a conventional source relaxed SiGe/strained Si heterojunction.

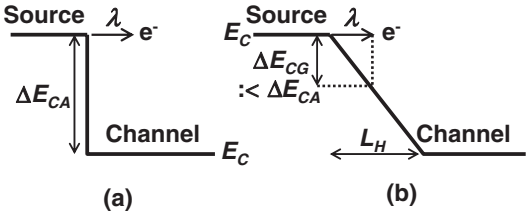

Fig. 2. Schematic of E_C profile of (a) abrupt and (b) linear graded source heterojunctions with the band offset of ΔE_{CA}. λ and L_H show the mean free path of inversion electrons and the graded region length of heterojunction, respectively. When $L_H > \lambda$, electrons can obtain a kinetic energy of only ΔE_{CG}.

band offset energy ΔE_{CA}. However, as shown in Fig. 2(b), when the mean free path λ of inversion electrons is shorter than the graded region length L_H of the source-heterojunction, electrons from the source region can obtain kinetic energy from only E_C drop energy ΔE_{CG} within the λ region at the source edge, which is smaller than ΔE_{CA} of the abrupt heterojunction. Namely, $\Delta E_{CG} < \Delta E_{CA}$. As a result, the increased electron velocity Δv_G [$\equiv (2\Delta E_{CG}/m_T^*)^{1/2}$] of linear graded source-heterojunctions is smaller than Δv_A [$\equiv (2\Delta E_{CA}/m_T^*)^{1/2}$] of abrupt heterojunction. Thus, the abrupt source-heterojunction is strongly needed.

Table I shows the best solutions of abrupt source heterostructures for CMOS-SHOTs. It is considered that these heterojunctions are not graded, because the diffusion of impurity atoms as in an alloy semiconductor and an element semiconductor does not occur in the new source heterojunction. In addition, a lower m_T^* of both electrons and holes can be realized in the strained Si and strained SiGe channel layers,[12] respectively. Table I also shows that the source conduction ΔE_C and the valence band offsets ΔE_V are nearly equal to the difference between the source and the channel energies. As a result, and as discussed in detail in Fig. 3, $\Delta E_C = E_C - \Delta_2$ and $\Delta E_V = HH - E_V$, where the channel energies of n- and p-MOSFETs are the energies of 2-fold valley (Δ_2) and the heavy hole band (HH) of the channel strained layers, respectively.

As shown in Fig. 3, we discuss new source heterojunction structures and the fabrication process. Figures 3(I) and 3(II) show new n-channel SHOT structures with source-relaxed Si/tensile-strained Si channel heterojunction and new p-channel SHOT structures with source-relaxed SiGe/compressive-strained SiGe channel heterojunction, respectively. The key process is the relaxation of the strained layers on the insulator owing to the slip between the strained layers and buried oxide (BOX) layers, by breaking the bonding between the strained and BOX layers using the recoil energy E_R of ions implanted into the interface. In this study, O^+ ions are selected, because of the neutral impurity in Si and the light mass. Therefore, it is necessary that $E_E + E_R > E_B$, where E_E and E_B are the elastic energy of strained substrates and the bonding energy between the strained and BOX layers, respectively. As shown in Figs. 3(I)(a) and 3(II)(a), after forming MOS structures on the strained semiconductor on insulator substrates, O^+ ion implantation into the source region as a mask of the gate electrode is carried out. In this work, Figs. 3(I)(b) and 3(II)(b) show the annealing process at 950 °C for 30 min to recover the crystallinity of the implanted region. As a result, only the source region is relaxed, resulting in the formation of relaxed-/strained-semiconductor heterojunction structures at the source region. Therefore, the conduction and the valence band energies of the source regions are shifted, as shown as the schematic band profiles in Figs. 3(I) and 3(II). ΔE_C (meV) and ΔE_V (meV) can be expressed as[14]

$$\Delta E_C = E_C - \Delta_2 = 134\Delta\varepsilon, \quad (1a)$$

$$\Delta E_V = HH - E_V = 0.77xR, \quad (1b)$$

where $\Delta\varepsilon$ is the strain difference (%) between the source and the channel region of strained Si layers and R is the relaxation rate (%) of strained $Si_{1-x}Ge_x$ layers caused by local O^+ ion implantation. The graded region L_H of the source heterojunction shown in Fig. 2 can be reduced, because of the very small lateral straggle $\Delta R_\perp$ of O^+ ions. On the other hand, the drain heterojunction causes the reduction in the drain current capability of SHOTs.[15] In addition, the drain energy spike also induces the backscattering of electrons,[16] resulting in the reduction in drain current drivability. Thus, Fig. 3(III) shows that the oblique O^+ implantation process is a key technique to prevent drain heterojunction formation near the drain pn junction, using the shadowing effects of the gate electrode at the inclined angle θ of O^+ ions whose implantation offset is $T_G \tan\theta$.

Here, E_R at the BOX interface should be high, but E_R in the strained layers should be as small as possible to suppress defect generation in the strained layer. Therefore, we have determined the O^+ ion implantation conditions of the dose D_O and the acceleration energy E_A, using a Monte Carlo simulator of ion implantation; stopping and range of ions in matter (SRIM).[17] Figures 4(a) and 4(b) show SRIM simulation results of recoil energy E_{R0} distribution for one O^+ ion and O^+ ion density profile in 60-nm-thick SSOI and 20-nm-thick SGOI substrates, respectively. We have successfully optimized the O^+ ion implantation conditions in both SSOIs and SGOIs such that E_{R0} peak is at approximately the strained layer/BOX interface, whose depth is equal to approximately $0.6R_P$ (R_P is the projected range of O^+ ion), and rapidly deceases in the strained semiconductor layers. Total E_R at the BOX interface is calculated to be $D_O E_{R0} \Delta x$, where Δx is the Si atom monolayer thickness at the BOX interface.

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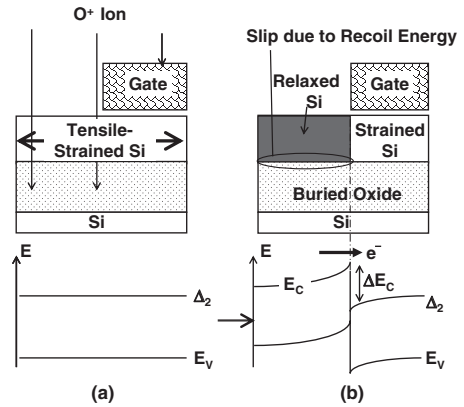
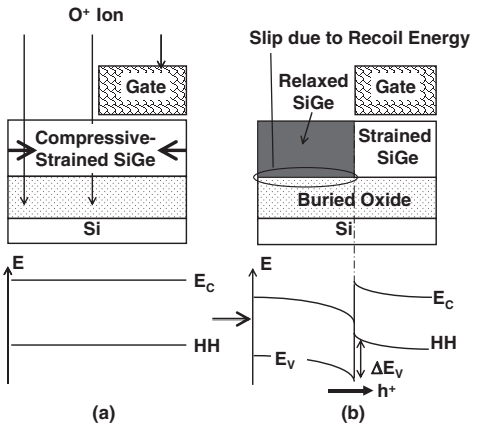
Table I. Source/channel abrupt heterostructures for n- and p-MOSFETs fabricated by SSOI and SGOI substrates in this study. The source energies of n- and p-MOSFETs are the conduction energy (E_C) and valence band energy (E_V) of the source relaxed layers, respectively. In addition, the channel energies of n- and p-MOSFETs are the energies of 2-fold valley (Δ_2) and the heavy hole band (HH) of the channel strained layers, respectively.

Device	Substrate	Source	Source energy	Channel	Channel energy
n-MOS	SSOI	Relaxed Si	E_C	Tensile-strained Si	Δ_2
p-MOS	SGOI	Relaxed SiGe	E_V	Compressive-strained SiGe	HH



(I)



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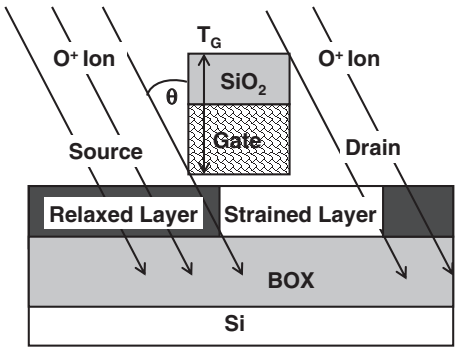
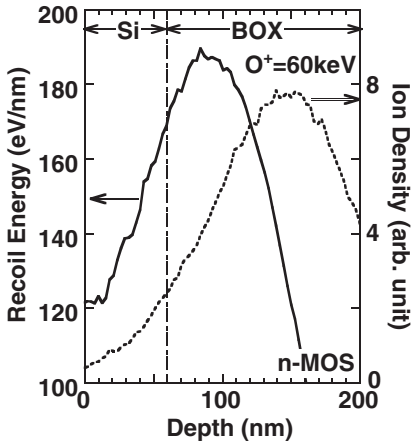
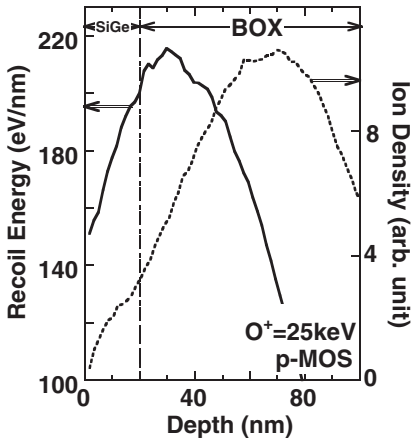


(III)

Fig. 3. (I) New n-channel SHOT structures with relaxed Si source/tensile-strained Si channel heterojunction and (II) new p-channel SHOT structures with source-relaxed SiGe/compressive-strained SiGe channel heterojunction fabricated by source O^+ ion implantation. Process steps in this study are follows: (a) After forming MOS structures on the strained layers on insulator substrates, O^+ ions are implanted into the source region as a mask of the gate electrode. (b) Furnace annealing at 950 °C for 30 min is carried out to recover the crystallinity of the implanted area. (III) The oblique O^+ implantation process is a key technique to prevent drain heterojunction formation near the pn junction.



(a)



(b)

Fig. 4. SRIM simulation results of recoil energy (solid lines) due to one O^+ ion E_{R0} and O^+ ion density profile (dashed lines) in (a) 60-nm-thick SSOI and (b) 20-nm-thick SGOI substrates. The O^+ ion energies for SSOIs and SGOIs are 60 and 25 keV, respectively.

In this experiment, as shown in Fig. 3, we have carried out furnace annealing for 30 min at 950 °C after O^+ ion implantation into a large area (1 cm^2) of strained substrates with a deposited 15-nm-thick surface oxide. The initial conditions of the strained substrates are as follows: 60-nm-thick SSOIs fabricated by wafer-bonding technology[18] and 20-nm-thick SGOIs with a Ge content of 28% formed by a Ge condensation technique[19] have a tensile strain of 0.7% and a fully compressive strain of 1.1%, respectively.

3. Relaxation of SSOIs and SGOIs Owing to O^+ Ion Implantation

In order to analyze the stress of very thin strained substrates, we have carried out UV/visible Raman spectroscopy using a 325 nm excitation wavelength He–Cd laser for SSOIs as well

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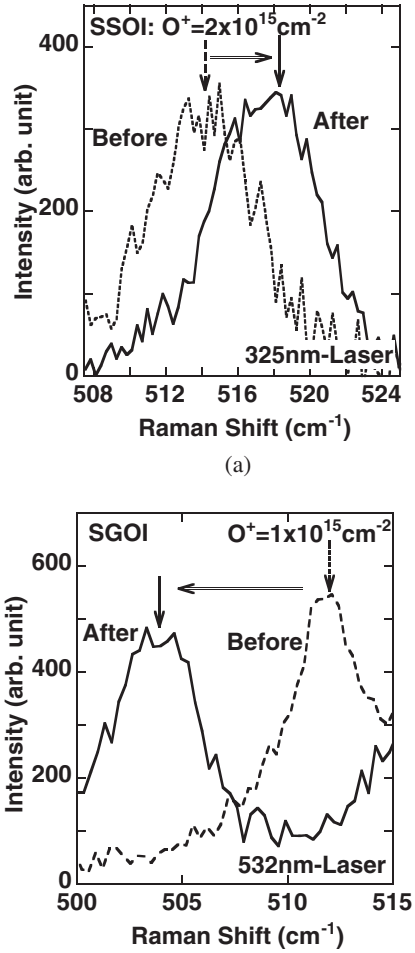

Fig. 5. Raman shift data of (a) SSOIs and (b) SGOIs before (dashed lines) and after (solid lines) O^+ ion implantation, obtained using (a) 325 nm wavelength He–Cd laser and (b) 532 nm wavelength green laser. (a) $T_{SSOI} = 60$ nm, $D_O = 2 \times 10^{15}$ cm^{-2}, and $E_A = 60$ keV. (b) $T_{SGOI} = 20$ nm, $D_O = 1 \times 10^{15}$ cm^{-2}, and $E_A = 25$ keV.

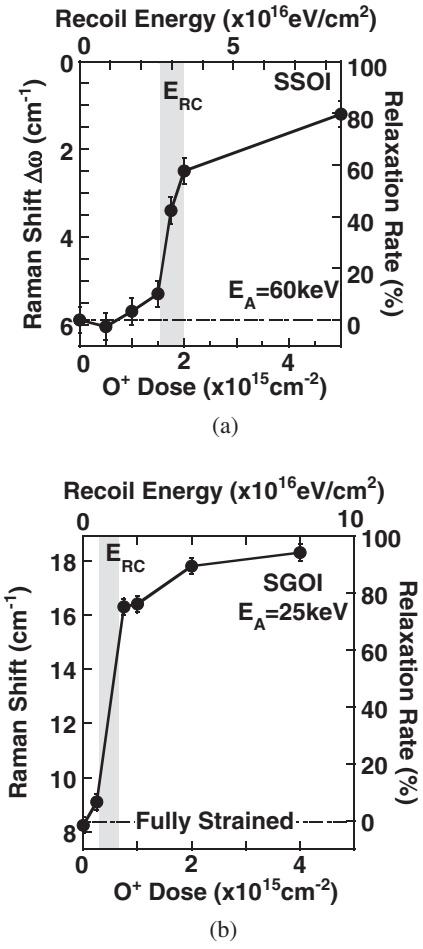

Fig. 6. Raman peak shift $\Delta\omega$ from the relaxed Si peak (520 cm^{-1}) and relaxation rate evaluated using $\Delta\omega$ of (a) SSOIs and (b) SGOIs versus O^+ ion dose. (a) $T_{SSOI} = 60$ nm and $E_A = 60$ keV. (b) $T_{SGOI} = 20$ nm and $E_A = 25$ keV. The upper axis indicates simulated recoil energy to the monolayer at the BOX interface. The shadow regions show the critical dose and E_R to relax the SSOIs and SGOIs.

as a 523 nm green laser for SGOIs. The penetration lengths of the 325 nm and the 532 nm lasers in Si are estimated to be about 5 nm and 1 μm, respectively. As a result, using the 325 nm laser, we can measure only the Raman peak due to the very thin strained Si, instead of the Si layer beneath the BOX layer.

Figure 5 shows the Raman shift data of SSOIs and SGOIs before (dashed lines) and after (solid lines) O^+ ion implantation. It is clear that the Raman peaks of both strained Si and SiGe layers shift toward the relaxed layer peak after O^+ ion implantation. Moreover, the half width of the SSOI and SGOI peaks, which is the barometer of the crystallinity, does not increase even after O^+ ion implantation, which indicates that the crystallinity of the implanted layers is not degraded.

Relaxation rate R of SSOIs and SGOIs can be evaluated from the experimental results of the Raman peak shift $\Delta\omega$ from the peak of relaxed Si (520 cm^{-1}) as

$$R = \begin{cases} \dfrac{\Delta\omega_{SS} - \Delta\omega}{\Delta\omega_{SS}} & \text{SSOI}, \\ \dfrac{\Delta\omega - \Delta\omega_{SG}}{\Delta\omega_R - \Delta\omega_{SG}} & \text{SGOI}, \end{cases} \quad (2)$$

where $\Delta\omega_{SS}$ and $\Delta\omega_{SG}$ are the Raman shift of the initial SSOIs and SGOIs, respectively, and $\Delta\omega_R$ is the ideal Raman shift of fully relaxed SGOIs. Figures 6(a) and 6(b) show $\Delta\omega$ and R of SSOIs and SGOIs as a function of D_O, respectively. The upper axis indicates the E_R simulated by SRIM. It is noted that the relaxation rate of both SSOIs and SGOIs suddenly increases at approximately the critical dose D_{CR} of O^+ ions which is indicated by a shadow, and then slowly increases with increasing D_O. However, SSOIs are still strained at $D_O \leq D_{CR}$. This result strongly suggests the presence of an abrupt lateral stress profile at the gate mask edge; thus, it is expected that the abrupt source heterojunction can easily be realized. The critical dose D_{CR} indicates the critical recoil energy E_{RC} to relax the strained layers. Consequently, we have experimentally demonstrated that both SSOIs and SGOIs can be relaxed by O^+ ion implantation.

We have carried out transmission electron microscopy (TEM) of a cross section of SSOIs at D_{CR} and higher dose conditions. Figure 7 shows TEM images of SSOIs. At D_{CR} of 2×10^{15} cm^{-2}, TEM shows a good quality of SSOIs even after O^+ ion implantation. The threading dislocation density of approximately 10^7 cm^{-2} can be achieved, which can be

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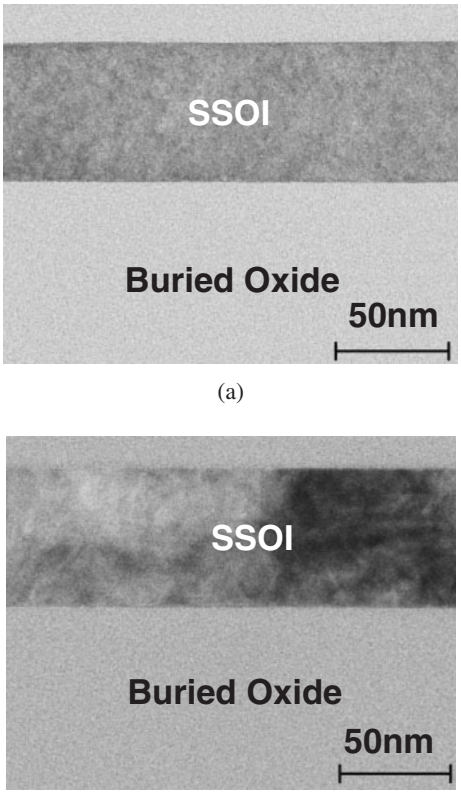

Fig. 7. TEM photos of cross section of relaxed SSOIs after O^+ ion implantation. (a) $D_O = 2 \times 10^{15}\,cm^{-2}$ of critical O^+ dose and (b) $D_O = 5 \times 10^{15}\,cm^{-2}$.

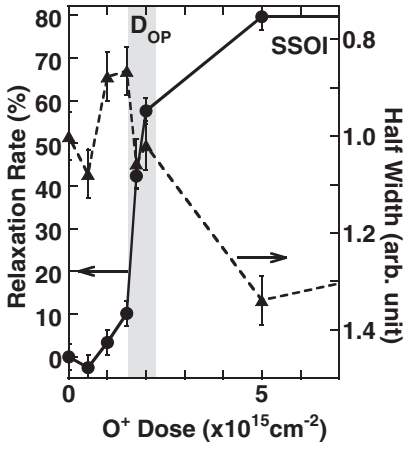

Fig. 8. Relaxation rate (solid line) of SSOIs evaluated from Raman shift and the half width of Raman peaks (dashed line) as a function of D_O, at the same ion implantation conditions in Fig. 6. The shadow region shows the optimized O^+ dose to relax the SSOIs.

reduced by optimizing the process conditions, such as the annealing process. However, we have observed the poly-crystallized SSOIs at higher D_O. Figure 8 shows the R (solid line) and half width (dashed line) of SSOIs as a function of D_O, at the same ion implantation conditions as those for the data shown in Fig. 6. The half width increases with increasing D_O. As a result, at approximately the critical dose D_{CR} indicated by a shadow, it is note that SSOIs can be relaxed without degrading the half width or the crystallinity of semiconductor layers. Therefore, it is concluded that

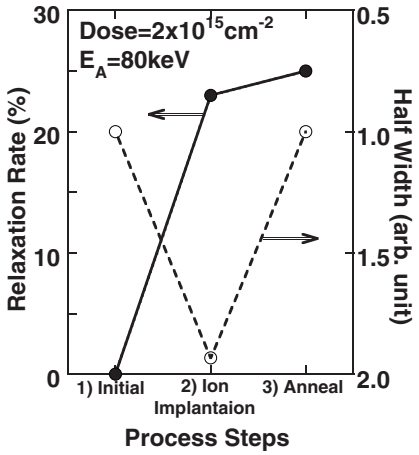

Fig. 9. Relaxation rate (solid line) of SSOIs evaluated from Raman shift and the half width of Raman peaks (dashed line) after each process step, where $T_{SSOI} = 60\,nm$, $D_O = 2 \times 10^{15}\,cm^{-2}$ and $E_A = 80\,keV$.

D_{CR} is the optimized O^+ ion implantation condition in this study.

Figure 9 shows the R (solid line) and half width of Raman peaks (dashed line) of SSOIs after each process step. The strained substrates are relaxed immediately after the O^+ ion implantation process, and R remains nearly constant even after annealing. On the other hand, the half width increases after O^+ ion implantation, but recovers after annealing. Therefore, the relaxation of strained layers is realized by only the O^+ ion implantation process and is not affected by the annealing process, and the crystallinity is recovered by the annealing process.

Next, we discuss the ion energy E_A dependence of R in SSOIs at a constant O^+ ion dose. Figure 10(a) shows the SRIM simulation results of the E_R profile as a function of E_A. E_R at the BOX interface increases with decreasing E_A. As a result, as shown in Fig. 10(b), the R of SSOIs rapidly decreases with increasing E_A, as expected.

Here, we summarize the relaxation rates of both SSOIs and SGOIs in various O^+ ion implantation conditions. Figure 11 shows R versus the recoil energy E_R at the BOX interface. In both SSOIs and SGOIs, we can obtain a universal relationship between R and E_R even under various O^+ ion implantation conditions. This is direct evidence that the strained substrates are relaxed by the recoil energy at the BOX interface. Furthermore, both SSOIs and SGOIs are suddenly relaxed at critical E_R. The critical E_R, $E_C{}^S$ for SSOIs, is about $3 \times 10^{16}\,eV/cm^2$ and is about 3 times higher than the critical E_R, $E_C{}^{SG}$ for SGOIs. The physical mechanism for the difference between $E_C{}^S$ and $E_C{}^{SG}$ is not understood now, but is considered to be due to the smaller bonding energy between the SiGe and BOX layers. In addition, $E_C{}^S$ is much higher than the bonding energy ($\sim 2 \times 10^{15}\,eV/cm^2$)[20,21] between the Si and buried oxide layers in SOI wafers bonded at 800 °C. This is due to the fact that bonding energy increases with increasing bonding temperature, and that the SSOI and SGOI wafers in this study are fabricated by a high-temperature bonding process. As shown in Fig. 8, it is concluded that the critical E_R condition is the optimal O^+ ion implantation condition for relaxing strained layers without polycrystallizing the strained layers.

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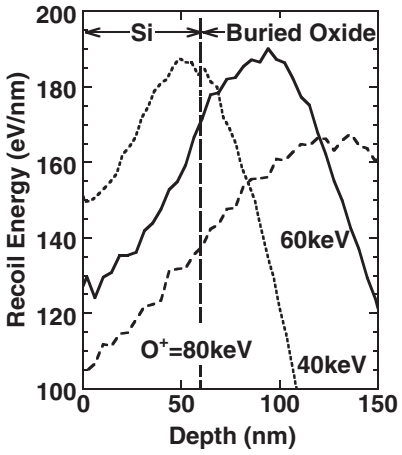
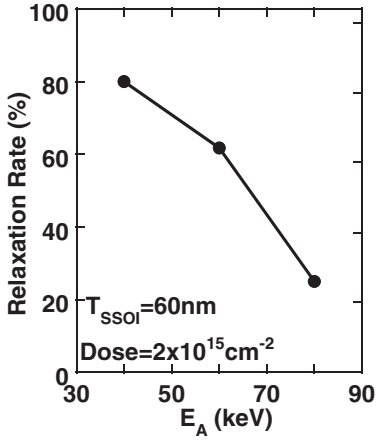


(a)



(b)

Fig. 10. (a) SRIM simulation results of E_R profile at various E_A values ($40 \leq E_A \leq 80$ keV) and constant D_O of 2×10^{15} cm^{-2} and (b) relaxation rate of SSOIs determined by Raman shift data (solid lines), where $T_{SSOI} = 60$ nm.

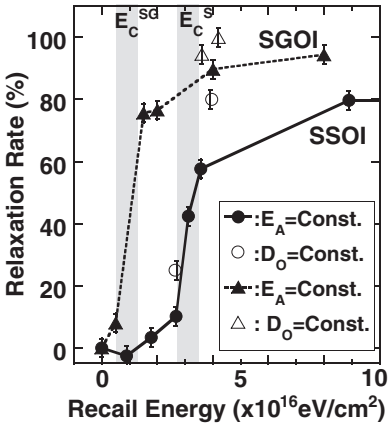


Fig. 11. Relaxation rate of SSOIs and SGOIs evaluated from Raman shift as a function of E_R at various O^+ ion doses and ion energies. Circles and triangles show the data of SSOIs and SGOIs, respectively. Closed and open characters show results under fixed E_A and fixed D_O conditions, respectively. The shadow regions indicate the critical recoil energy for relaxing SSOIs (E_C^S) and SGOIs (E_C^{SG}).

According to eqs. (1) and (2), we can estimate the band offset energies at the source heterojunction. At the critical E_R conditions, the ΔE_C in SSOIs and ΔE_V in SGOIs in this work are estimated to be about 70 and 160 meV, respectively. In order to realize much higher ΔE_C and ΔE_V, it is necessary to increase the initial strain values of the strained substrates.

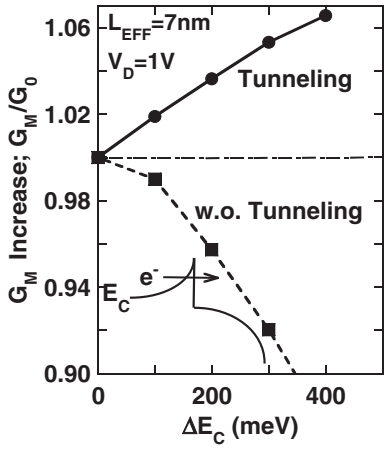


Fig. 12. Simulated enhancement factors for maximum G_M of n-channel SHOTs with abrupt heterojunction G_M/G_0 as a function of ΔE_C, where G_0 is the maximum G_M value at ΔE_C of 0 eV, $L_{EFF} = 7$ nm, $T_{OX} = 1$ nm, $T_{SOI} = 3$ nm, $T_{BOX} = 10$ nm, and $V_D = 1$ V. The solid and dashed lines show the results of simulation with and without considering tunneling effects of electrons at the energy spike of the source heterojunction. The inset shows schematic tunneling effects of electrons at the energy spike.

4. Simulation of SHOT Performance at Sub-10 nm Regime

Using a two-dimensional (2D) device simulator[22] with a drift diffusion model considering the tunnel effects of electrons[23] at the energy spike of the source heterojunction in n-SHOTs with an abrupt source heterojunction as well as the quantum confinement effects of electrons in thin SOI stuctures, we discuss the transconductance G_M peak increase ΔG_M in SHOTs with the effective channel length L_{EFF} of 7 nm. In order to suppress the short channel effects of SHOTs, it is assumed that the channel thickness T_{SOI} is 3 nm, the gate oxide thickness T_{OX} is 1 nm, the buried oxide layer thickness T_{BOX} is 10 nm, and the drain bias V_D is 1 V. Since the 2D device simulator adopts the drift diffusion model, it is noted that G_M itself and ΔG_M are underestimated. Figure 12 shows the G_M peak increase ΔG_M of SHOTs as a function of ΔE_C, with and without considering the tunnel effects of electrons at the source heterojunction. ΔG_M considering the tunnel effects continues to increase with increasing ΔE_C, although simulation results without the tunneling effects indicate the reduction of the G_M increase at high ΔE_C. The latter case is due to the higher resistance of the source energy spike at high ΔE_C. Therefore, the tunneling electrons at the source heterojunction are the key factors for realizing higher G_M. As a result, it is necessary to increase ΔE_C in order to realize higher performance in SHOTs.

Next, we discuss the simulation results of graded SHOTs. Figure 13 shows the simulation results with the tunneling effects of the dependence of the ΔG_M on L_H in linear graded heterojunction structures, where $\Delta E_C = 0.3$ eV. ΔG_M decreases with increasing L_H, which is also caused by both the decrease in the tunneling rate of electrons at larger L_H and

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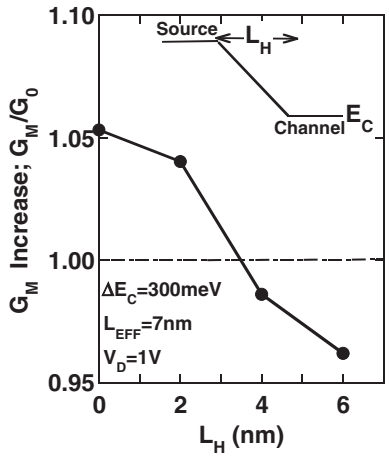

Fig. 13. Simulated enhancement factors of maximum G_M of graded SHOTs G_M/G_0 as a function of graded length L_H of source heterojunction shown in the inset, where $\Delta E_C = 0.3$ eV, $L_{EFF} = 7$ nm, and $V_D = 1$ V.

the physical mechanism mentioned in Fig. 2. Therefore, it is confirmed that the G_M performance of SHOTs is reduced in the case of a graded source heterojunction. Therefore, it is recognized that an abrupt source heterojunction is strongly needed.

5. Conclusions

We have experimentally studied novel abrupt source heterojunction structures for quasi-ballistic CMOS, using lateral relaxed/strained layers by controlling the local strain in SSOIs for n-MOS and SGOIs for p-MOS. The key technology in this study is to relax the strained layers using O^+ ion implantation recoil energy in the BOX interface. From the Raman analysis of the SSOIs and SGOIs, we have successfully relaxed both the SSOI and SGOI substrates without polycrystallizing the substrates. Moreover, we have experimentally confirmed the critical recoil energy at the BOX interface to relax the strained substrates, and both the SSOI and SGOI substrates are suddenly relaxed at the critical recoil energy, which suggests that an abrupt heterojunction will be achieved by the O^+ ion implantation technique. We have obtained the universal relationship between the relaxation rate of the strained layers and the recoil energy at the BOX interface under various O^+ ion implantation conditions. As a result, the source band offset ΔE_C and ΔE_V can be controlled by O^+ ion implantation conditions. The results of simulation considering the tunnel effects at the source heterojunction indicate that the increase in G_M of sub-10 nm SHOTs continues with increasing ΔE_C. Consequently, SHOT structures with the novel abrupt source heterojunction are very promising for future quasi-ballistic CMOS devices.

Acknowledgement

We would like to thank Professor J. Nakata and Dr. Y. Hoshino of Kanagawa University for ion implantation technology and Dr. T. Kanayama for continuous support. This work was partially supported by a Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology (20035014), a Grant-in-Aid for Scientific Research from the Japan Society for the Promotion of Science (21560371), and NEDO.

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