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Characterization of polycrystalline silicon thin films fabricated by rapid joule heating method

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ABSTRACT Polycrystalline thin film transistors (poly-Si TFTs) were fabricated using the 5-μs-rapid joule heating method. The optimum condition of 0.77 J/cm^2 for crystallization was determined through analysis of transfer characteristics of poly-Si TFTs. The density of the tail-type defect states decreased from 1.4×10^{12} to 9.5×10^{11} cm^{-2} and the carrier mobility increased from 300 cm^2/Vs to 760 cm^2/Vs as the joule heating energy density increased from 0.68 to 0.77 J/cm^2. The threshold voltage of the drain current ranged between 0.9 and 1.15 V.

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1 Introduction

Rapid thermal annealing is an attractive method for fabrication of polycrystalline silicon thin film transistors (poly-Si TFTs) at a low cost due to the low thermal budget process [1–5]. Laser crystallization, for example, has been widely used. Polycrystalline silicon films with a high crystalline volume ratio are formed on glass substrates at room temperature atmosphere. Fabrication of poly-Si TFTs with high carrier mobility has been achieved. We have recently developed the electrical-current-induced joule heating as a simple and rapid thermal annealing method [6–8]. Crystallization of silicon films has been achieved through micro-second order rapid heating of silicon films caused by electrical-current-induced joule heating. A high carrier mobility of ∼ 570 cm^2/Vs and a low threshold voltage of ∼ 1.8 V have been demonstrated [8].

In this paper, we report fabrication and analysis of poly-Si TFTs fabricated in the polycrystalline silicon films formed by the rapid joule heating. The analysis shows that the poly-Si films have tail-type defect states. We discuss effective carrier mobility and the effective threshold voltage for TFTs with tail-type defect states in the channel region. We report that the density of defect states decreases as the joule heating energy density increases and that the effective carrier mobility increases to 760 cm^2/Vs.

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2 Fabrication of poly-Si TFTs

Figure 1 shows the fabrication steps of poly-Si TFTs. 50-nm-thick undoped amorphous silicon films were formed on glass substrates. 200-nm-thick SiO_x islands with a length of 25 μm and a width of 70 μm were formed on channel regions of the silicon films as the dopant stopper. Phosphorus atoms were implanted at 10 keV with a density of 1.6×10^{15} cm^{-2}. After removing the dopant-stopper-SiO_2 islands, crystallization and dopant activation were simultaneously carried out with the joule heating method [6, 7]. For joule heating, 300-nm-thick SiO_2 intermediate films were formed on the silicon films. 100-nm-thick chromium strips with a width of 200 μm and a length of 500 μm were then defined on SiO_2 above the channel regions. Voltages with a pulse width of 5 μs were applied to the chromium strips. The joule heat energy generated at chromium strips diffused to underly-

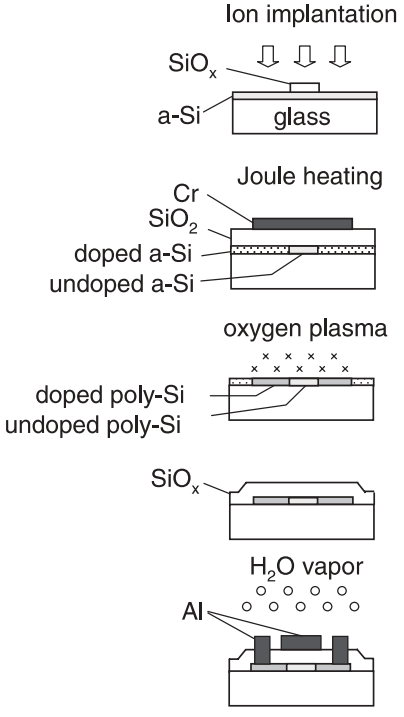

FIGURE 1 Schematic fabrication flow of poly-Si TFTs

ing layer and the silicon films are heated by heat flow through the intermediate SiO_2 layer. The crystallization threshold energy density of silicon films was $0.60\,J/cm^2$ at 115 V for 5-μs-pulsed voltage application. Observation of transmission electron microscope (TEM) revealed that the silicon region underlying the chromium strips was completely crystallized. Crystalline grains were formed with an average size of 200 nm at $0.77\,J/cm^2$ for 5-μs-joule heating.

In the TFT fabrication, the silicon channel regions and source and drain regions below the chromium strips were successfully crystallized at energies from $0.68 \sim 0.77\,J/cm^2$ with no substrate heating. The dopant atoms in the source and drain regions below the chromium strips were also activated. After removing the SiO_2 layers and the chromium strips, 13.56 MHz-remote-type-oxygen plasma at 100 W, 130 Pa and 250 °C for 30 min was applied to oxidize dangling bonds [9]. Silicon islands were then defined. SiO_2 films $130 \sim 150$-nm-thick were then formed as the gate insulator by thermal evaporation of SiO powders in the oxygen radical atmosphere at room temperature [10]. Contact holes were opened and then Al gate, source and drain electrodes were formed. After fabrication of the TFT structure, TFTs were heated at 200 °C with 1.3×10^6 Pa H_2O vapor for 3 h for improvement SiO_2 properties [11, 12]. The capacitance response with the gate voltage with a frequency of 1 MHz for Al gate metal-oxide-semiconductor (MOS) capacitors was analyzed. The specific dielectric constant of the SiO_2 layer, the densities of interface traps and fixed oxide charges were estimated to be 4.9, $2.0 \times 10^{10}\,cm^{-2}eV^{-1}$ and $3.4 \times 10^{10}\,cm^{-2}$, respectively, after H_2O vapor heat the treatment at 200 °C with 1.3×10^6 Pa H_2O vapor for 3 h.

3 Analysis of TFT transfer characteristics

In order to estimate the density of defect states in polycrystalline silicon of the poly-Si TFTs, we developed a numerical calculation program used with finite-element method combined with statistical thermodynamical conditions with defect states localized at SiO_2/Si interfaces as well as silicon films [10, 13]. The defect states were placed spatial-uniformly in the silicon films. We used two types of defects. One is the deep level defect localized at the mid gap, whose density distributes as the Gaussian function in the band gap. The other one is the tail-type defect, whose density exponentially decreased from the band edge to the mid gap. The density of defect states at SiO_2/Si interfaces was determined by *C–V* measurements of MOS capacitors. The carrier scattering factor at grain boundaries was also introduced to the calculation program. Because lattice orientation changes at grain boundaries, electron carriers can be scattered at grain boundaries and the carrier mobility is reduced compared with single crystalline silicon. Carrier scattering due to phonon, ionized impurity, charged defects were also introduced. Phonon scattering depends on the electrical field at the inversion layer [14, 15]. The phonon scattering rate increases and the carrier mobility decreases as the gate voltage increases. Ionized impurities and charged-up defects also cause coulomb scattering and reduce the carrier mobility.

We analyzed the linear relation of transfer characteristics with a small drain voltage of 0.1 V. The best agreement of calculated transfer characteristics to experimental ones resulted in the free carrier density, the carrier mobility, the density of defect states. Figure 2a shows calculated drain current as a function of the gate voltage for tail-type defect states with a width of 0.15 eV and a density of $1.0 \times 10^{12}\,cm^{-2}$. Although the drain current increased with low gate voltage application, a gate voltage of about 1.0 V was necessary to increase the drain current high enough because of carrier trapping by defects. The problem is the drain current does not linearly increase by increasing the gate voltage in the case of the tail-type defects, as shown in Fig. 2a. The drain current gradually increases so that the threshold voltage of the drain current is not well defined from the linear relation with drain current and gate voltage. When the drain voltage is much lower than the gate voltage (linear region), the drain current is given by

$$I_d = \frac{W}{L} e V_d \int_0^d n(x, V_g)\mu(x, V_g)\mathrm{d}x\,, \qquad (1)$$

where W and L are the width and length of the channel, e is the elemental charge, V_d is the drain voltage, d is the film thick-

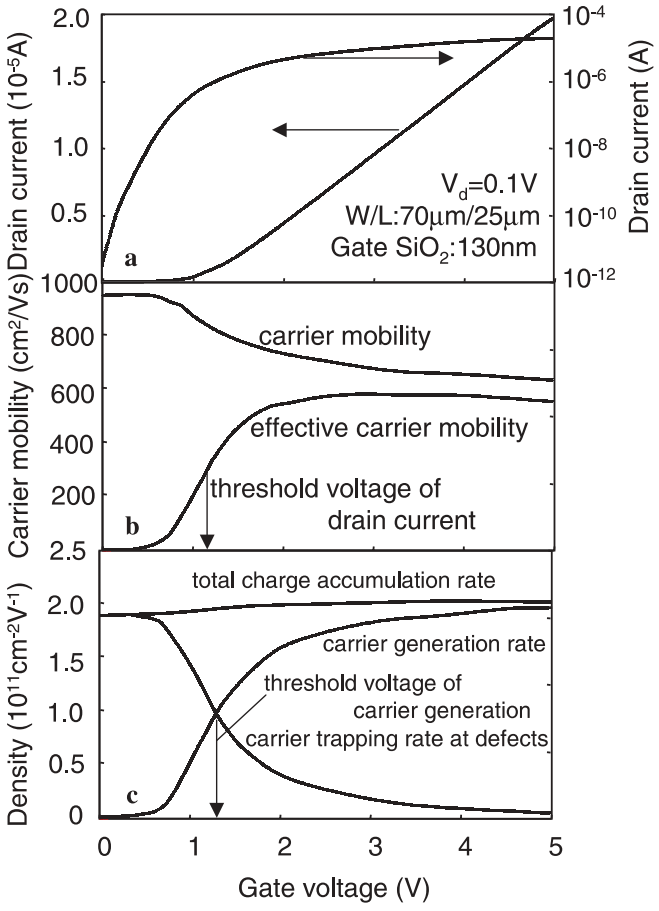

FIGURE 2 Calculated drain current as a function of the gate voltage for a TFT with a tail-type defect density of $1.0 \times 10^{12}\,cm^{-2}$ and a width of 0.15 eV (**a**), intrinsic carrier mobility and effective carrier mobility as a function of the gate voltage (**b**), and the free carrier generation rate, the carrier trapping rate at defects and their summation as a function of the gate voltage (**c**). The threshold voltages of the drain current and of carrier generation are presented by *arrows* in **b** and **c**, respectively

ness, $n(x, V_g)$ is the carrier volume density and $\mu(x, V_g)$ is the carrier mobility as functions of the depth x and the gate voltage V_g. We defined the threshold voltage of the drain current as a voltage at a half of the maximum transconductance, g_m ($=\frac{\partial I_d}{\partial V_g}$). The g_m is given as,

$$g_m = \frac{W}{L} e V_d \int_0^d \left(\frac{\partial n(x, V_g)}{\partial V_g} \mu(x, V_g) + n(x, V_g) \frac{\partial \mu(x, V_g)}{\partial V_g} \right) dx \tag{2}$$

The g_m also gives the effective carrier mobility as,

$$\mu_{eff} = g_m \left(\frac{W}{L} C_{ox} V_d \right)^{-1} = \frac{e}{C_{ox}} \int_0^d \left(\frac{\partial n(x, V_g)}{\partial V_g} \mu(x, V_g) + n(x, V_g) \frac{\partial \mu(x, V_g)}{\partial V_g} \right) dx , \tag{3}$$

where C_{ox} is the capacitance of the gate insulator.

Figure 2b shows the effective carrier mobility and real carrier mobility as a function of the gate voltage. The threshold voltage is also presented by an arrow at a half point of the maximum transconductance. The carrier mobility decreases due to the high phonon scattering effect as the gate voltage increases, as shown in Fig. 2b. Therefore $n(x, V_g)\frac{\partial \mu(x, V_g)}{\partial V_g}$ is negative in (2) and (3). Moreover, the carrier generation rate, $\frac{\partial n}{\partial V_g}$, is lower than the total charge generation rate, $\sim \frac{C_{ox}}{e}$, especially at low gate voltage region because of carrier trapping at defects. Therefore the effective carrier mobility is lower than the real carrier mobility, as shown in Fig. 2b.

Figure 2c shows the calculated free carrier generation rate, $\frac{\partial n}{\partial V_g}$, the carrier trapping rate at defects $\left|\frac{\partial N_t}{\partial V_g}\right|$, and their summation in the case of tail-type defect states with a width of 0.15 eV and a density of $1.0 \times 10^{12}\,cm^{-2}$, where N_t is the density of carriers trapped at defects per unit area. The free carrier generation rate was almost zero at the low gate voltage region because of serious carrier trapping at defect states. The free carrier generation rate gradually increased and the carrier trapping rate at defects gradually decreased as the gate voltage increased, as shown in Fig. 2c. The threshold voltage of carrier generation should be defined as the voltage at which the both rates coincide with each other as shown by an arrow in Fig. 2c. Above the threshold voltage, the free carrier generation rate is higher than the charge trapping rate at defects. The carrier trapping rate at defects decreased to almost zero with enough high gate voltage. The carrier mobility decreases due to the phonon scattering effect as the gate voltage increases and $n(x, V_g)\frac{\partial \mu(x, V_g)}{\partial V_g}$ is negative, as shown in Fig. 2b and (2). Therefore, the threshold voltage of the drain current obtained from g_m is lower than the threshold voltage of carrier generation, as shown in Fig. 2b and c. The summation of the free carrier generation rate and the carrier trapping rate at defects was almost constant and equal to the density of charge accumulated at the gate electrode. It increased slightly as the gate voltage increased, as shown in Fig. 2c. The ratio of the-silicon-surface-potential/the-gate-voltage decreased as the gate voltage increased because the electrical resistivity of the silicon layer decreased due to electron carrier accumulation so that the gate voltage is effectively applied to the SiO_2 gate insulator and the charge generation rate increased for high the gate voltage application.

4 Results and discussion

Figure 3 shows experimental transfer characteristics of the *n*-channel poly-Si TFTs for crystallization with the joule heating energy density from $0.69 \sim 0.77\,J/cm^2$ (solid curves). A sharp increase in the drain current with low gate voltage application was observed. The drain current increased as the joule heating energy density increased. Dashed curves shown in Fig. 3 are calculated transfer characteristics best fitted to experimental curves. The analysis revealed that the calculated drain current agreed well with experimental ones when tail-type-defect state was used. Figure 4 shows the total density of tail-type defect states (a) and the width of the tail states (b) as a function of the joule heating energy density. The defect density slightly decreased from 1.3×10^{12} to $9.5 \times 10^{11}\,cm^{-2}$ as the joule heating energy density increased from 0.68 to $0.77\,J/cm^2$. The width of the tail state ranged from 0.12 to 0.15 eV. It slightly increased as the joule heating energy density increased.

Figure 5 shows the threshold voltage of the drain current (a) and the effective carrier mobility (b) as a function of the joule heating energy density. The threshold voltage of the drain current distributed between 0.9 and 1.15 V. The low threshold voltage resulted from the low density of defect states at the deep energy level region. It was almost independent of the joule heating energy density. Figure 5a also shows the threshold voltage of carrier generation. It was $0.1 \sim 0.2$ V higher than the threshold voltage of the drain current. The difference between the threshold voltages was caused by the fact that the carrier mobility decreased with increasing the gate voltage. The threshold voltage of carrier generation was

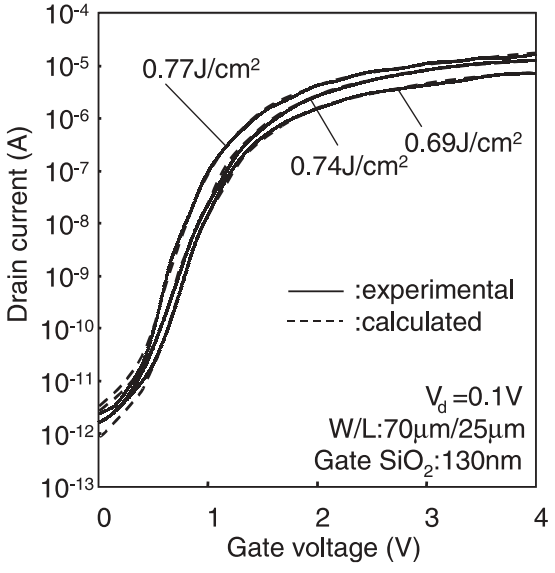

FIGURE 3 Transfer characteristics of *n*-channel poly-Si TFTs fabricated at joule heating energy densities at 0.69 ,0.74 and $0.77\,J/cm^2$, respectively (*solid curve*). The calculated drain current is also presented by *dashed curve* for each joule heating energy density (*dashed curve*)

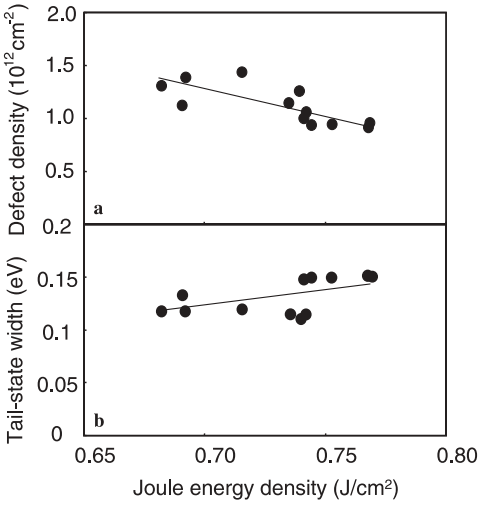

FIGURE 4 The density of tail-type-defect states (**a**) and the width of the tail-type defects (**b**) as a function of the joule heating energy density

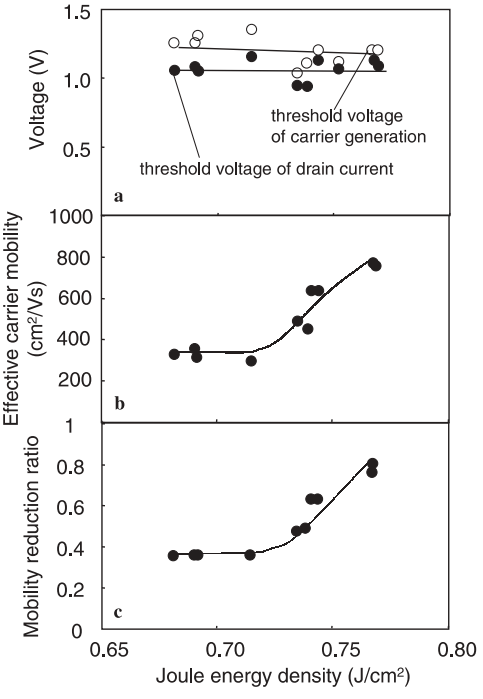

FIGURE 5 The threshold voltages of the drain current and carrier generation as a function of the joule heating energy density (**a**), the effective carrier mobility (**b**), and the mobility reduction factor due to carrier scattering (**c**) as functions of the joule heating energy density

also almost independent of the joule heating energy density. This means that the density of defect states at deep energy region in the band gap was almost same for every joule heating energy case. Our calculation resulted in that $2.1 \times 10^{11} \sim 2.6 \times 10^{11}$ cm^{-2} defect states were located from the mid gap to the Fermi level (~ 0.96 eV from the valence edge) which gave the threshold voltage of the carrier generation. Defect reduction processes of the oxygen plasma and high-pressure H_2O vapor was important to effectively reduce dangling bond which caused deep level defect states. On the other hand the defect density from the Fermi level to the conduction edge decreased from 1.0×10^{12} to 7.4×10^{11} cm^{-2} as the joule heating energy density increased from 0.68 to 0.77 J/cm^2. The high joule heating energy density was important for reducing the tail-type defect density near conduction band edge.

The maximum effective carrier mobility increased from 300 to 760 cm^2/Vs, as the joule heating energy density increased from 0.68 to 0.77 J/cm^2, as shown in Fig. 5b. The low density of defect states near conduction band for the high joule heating energy density resulted in the high g_m and the high effective mobility. Moreover, our numerical analysis revealed that the carrier scattering rate at the grain boundary markedly changed with the joule heating energy density. The mobility reduction coefficient is seriously low in the conditions of the low joule heating energy densities as shown in Fig. 5c due to the carrier scattering. The reduction coefficient increased from 0.37 to 0.80 as the joule heating energy density increased from 0.68 to 0.77 J/cm^2, as shown in Fig. 5c. High mobility resulted from a low carrier scattering rate.

These results characterize electrical properties of the poly-Si films formed by the rapid joule-heating method. The threshold energy density for crystallization was 0.6 J/cm^2 for the present joule heating condition with 5 μs heating and the 300-nm-thick intermediate SiO_2 layer. Our previous study indicates that the silicon films are heated from room temperature to high temperature during the joule heating, and temperatures reached the melting point at voltage pulse termination, 5 μs, in the case of the threshold energy density of 0.6 J/cm^2 [7, 16]. Heating duration at high temperatures near or above the melting point markedly increases as the joule heating energy density above the threshold increases. We conducted one dimensional heat flow calculation, in order to estimate silicon heating by the 5-μs-joule heating. The calculation resulted in the heating of silicon films to the melting point at 4.0 μs and 3.6 μs after initiation of the joule heating for 0.68 and 0.77 J/cm^2 joule heating, respectively. Therefore heating duration at high temperature and the melting duration markedly increased to about 1 μs for the high joule heating energy density of ~ 0.77 J/cm^2. Analysis of the TFT transfer characteristics showed that the density of the tail-type defect and the carrier scattering degree were low for the high joule heating energy density increased, as shown in Figs. 4 and 5. These investigations indicate that micro-second melting and annealing duration at high temperature are important for improving electrical properties of polycrystalline silicon. The grain size will be increased and silicon bonding network at grain boundaries will be in thermally relaxation states. Silicon bonding distortion, the density of tail-type defect states and carrier scattering rate at grain boundaries will be reduced so that the effective carrier mobility increased.

5 Summary

Electrical properties of polycrystalline silicon thin films crystallized by the 5 μs-rapid joule heating method are precisely analyzed. *N*-channel poly-Si TFTs with a channel length of 25 μm and a width of 70 μm were fabricated with crystallization and dopant activation using the 5 μs rapid joule heating method. Analyses of transfer characteristics using a numerical calculation program using the finite-element method revealed that the poly-Si films had tail-type defects in the band gap. The defect density decreased from 1.3×10^{12} to 9.5×10^{11} cm^{-2} as the joule heating energy density increased

from 0.68 to 0.77 J/cm^2. On the other hand, the mobility reduction factor increased from 0.37 to 0.80. These resulted in a high effective carrier mobility of 760 cm^2/Vs and a low threshold voltage of the drain current of $0.9 \sim 1.15$ V. The long heating above the melting point longer than 1 μs was achieved by the 0.77 J/cm^2-joule heating for 5 μs. It probably made thermally relaxed silicon bonding network states at grain boundaries with a low density of defect sates and a low carrier scattering rate.

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