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Application of Rapid Joule Heating Method to Fabrication of Polycrystalline Silicon Thin Film Transistors

Toshiyuki SAMESHIMA, Yoshiyasu KANEKO and Nobuyuki ANDOH

Tokyo University of Agriculture and Technology, 2-24-16, Nakamachi, Koganei, Tokyo 184-8588, Japan

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We report the rapid crystallization of silicon films with a joule heating method and its application to the fabrication of n-channel and p-channel polycrystalline silicon thin film transistors (poly-Si TFTs). Crystallization of 50-nm-thick silicon films and activation of dopant atoms were successfully achieved by rapid heat diffusion via 300-nm-thick SiO_2 intermediate layers from joule heating induced by electrical current flowing in chromium strips. The average grain size was about 100 nm in crystallized films. A high electrical conductivity of 2050 S/cm was achieved for 1.3×10^{21}-cm^{-3}-phosphorus doped silicon films. TFTs have a carrier mobility and a threshold voltage of 570 cm^2/Vs and 1.8 V for n-channel TFTs, and 270 cm^2/Vs and −2.8 V for p-channel TFTs, respectively. [DOI: 10.1143/JJAP.42.5461]

KEYWORDS: joule heating, crystallization, poly-Si, TFT, defect, mobility

1. Introduction

Rapid thermal annealing is useful for the fabrication of polycrystalline silicon thin film transistors (poly-Si TFTs) at low processing temperatures and their application to electrical devices.[1–7] Laser crystallization has been widely used for the rapid formation of polycrystalline silicon films. Poly-Si TFTs with high carrier mobility have been achieved. However, complicated optical equipment is required in order to deliver the laser beam to samples and to control the distribution of laser beam intensity for laser crystallization. We have recently demonstrated a simple crystallization method using electrical-current-induced joule heating[8,9] and reported a possibility of poly-Si-TFT fabrication.[10] Microsecond order rapid heating is achieved by joule heating caused by electrical current flowing in thin metal films. Silicon films have been rapidly heated and crystallized via intermediate insulating layers. In this paper, we characterize the crystallization of silicon films using the rapid joule heating method. The behavior of dopant activation is also discussed. We report the fabrication of n-channel and p-channel polycrystalline silicon thin film transistors using the rapid crystallization and activation processes with the joule heating method. A high carrier mobility of 570 cm^2/Vs and a low threshold voltage of 1.8 V demonstrate that the polycrystalline silicon films fabricated by the present method have a device quality.

2. Experimental

Figure 1 shows a schematic apparatus of the present joule heating method for crystallization of silicon films. Amorphous silicon films with a thickness of 50 nm were formed on glass substrates. 300-nm-thick SiO_2 films were formed on the silicon films. 100-nm-thick chromium films were subsequently formed on the SiO_2 films. Chromium strips with a width of 200 μm and a length of 500 μm were defined above the channel regions. The resistance of the chromium strips was 65 Ω. Aluminum electrodes were formed at the edges of the chromium strips to apply electrical voltages. Voltages with pulse widths of 3 and 5 μs were applied to the samples. The electrical current was measured as a voltage V_1 at the 2.2-Ω load resistance R_1 connected between the sample and ground using a digital oscilloscope in order to obtain the joule heating intensity as shown in Fig. 1. The joule heating

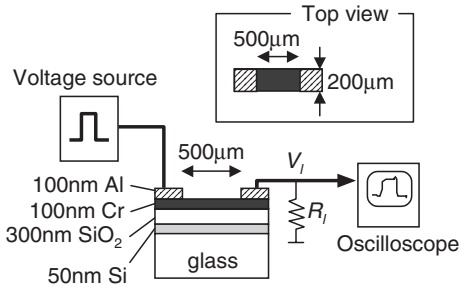

Fig. 1. Schematic apparatus of the rapid joule heating and the cross section of the layered structure of samples. 3 and 5-μs-pulsed voltages were applied to 100-nm thick Cr strip with a length of 500 μm and a width of 200 μm.

intensity per unit area $P(t)$ is given as

$$P(t) = \frac{\left(V_0 - V_l\left(1 + \frac{R_s}{R_l}\right)\right)V_l}{R_l S}, \quad (1)$$

where V_0 is the applied voltage, R_s is the series resistance, 10 Ω, of the circuit and S is the area of the chromium strips. The joule heat generated at the chromium films diffuses into the underlying layer and the silicon films are heated by the heat flow through the intermediate SiO_2 layer. A transmission electron microscope was used for investigating the distribution of crystalline grains. In order to investigate the activation behavior of dopant atoms in silicon films, especially at high doping concentration conditions, 3.3×10^{20}–1.3×10^{21}-cm^{-3}-phosphorus-doped amorphous silicon films with a thickness of 50 nm were formed by plasma enhanced chemical vapor deposition using mixed gases of SiH_4 and PH_3. Hall effect current measurement was carried out in order to estimate the electrical conductivity, the carrier mobility and the carrier density.

Figure 2 shows the fabrication steps of poly-Si TFTs. 50-nm-thick undoped amorphous silicon films were formed on glass substrates. 200-nm-thick SiO_x islands with a length of 25 μm and a width of 70 μm were formed on channel regions of the silicon films as the dopant stopper. Phosphorus and boron atoms were implanted at 10 KeV with a density of 1.3×10^{15} cm^{-2}. After removing the dopant-stopper-SiO_2 islands, crystallization and dopant activation were simulta-

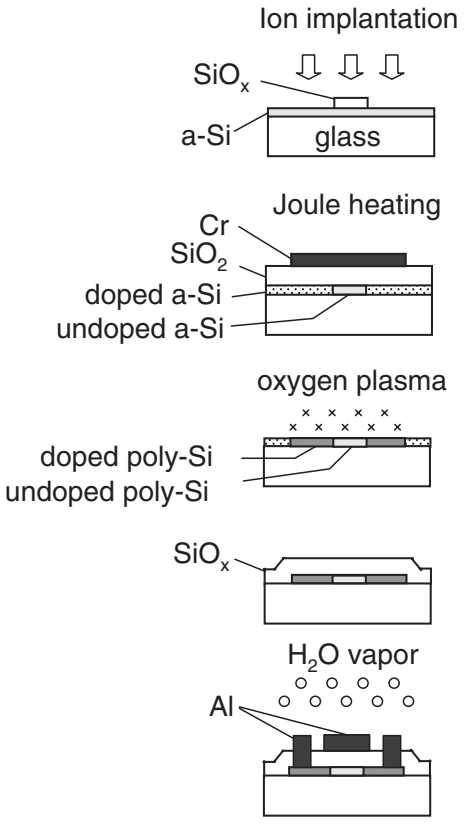

Fig. 2. Schematic fabrication flow of poly-Si TFTs.

neously carried out by the joule heating method, as shown in Fig. 1. The silicon channel regions and source drain regions below the chromium strips were successfully crystallized at energies from 0.6–0.78 J/cm^2 with no substrate heating. The dopant atoms in the source and drain regions below the chromium strips were also activated. After removing the SiO_2 layers and the Cr strips, 13.56 MHz-remote-type-oxygen plasma at 100 W, 130 Pa and 250°C for 30 min was applied for defect reduction in polycrystalline silicon films.[11] Silicon islands were then defined. SiO_x films 130–150-nm-thick were then formed as the gate insulator by thermal evaporation of SiO powders in the oxygen radical atmosphere at room temperature.[12] Contact holes were opened and then Al gate, source and drain electrodes were formed. After the fabrication of the TFT structure, TFTs were heated at 200°C using 1.3×10^6 Pa H_2O vapor for 3 h for improvement of SiO_x properties.[13,14] *C–V* measurement determined the dielectric constant of SiO_x and the density of interface trap states. The capacitance response with the gate voltage with a frequency of 1 MHz for Al gate metal–oxide–semiconductor (MOS) capacitors was analyzed. The specific dielectric constant of the SiO_x layer, the densities of interface traps and fixed oxide charges were estimated to be 4.9, 2.0×10^{10} cm^{-2}eV^{-1} and 3.4×10^{10} cm^{-2}, respectively, after H_2O vapor heat the treatment at 200°C using 1.3×10^6 Pa H_2O vapor for 3 h.

3. Results and Discussion

Figure 3 shows the joule heating energy density per unit area measured using the equipment shown in Fig. 1 as a function of voltages applied to the chromium strips for 3 and 5 μs. The joule heating energy density increased as the

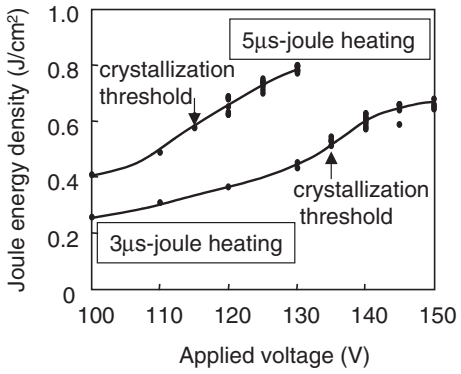

Fig. 3. Joule heating energy density per unit area as a function of voltages applied to the chromium strips for 3 and 5 μs. Solid circles indicate experimental points measured using the equipment shown in Fig. 1. The condition for crystallization threshold of silicon films is also represented.

applied voltage increased. The joule heat generated at the chromium films diffused into the underlying layer and the silicon films were heated by heat flow through the intermediate SiO_2 layer. Visual observation and Raman scattering measurements determined that the crystallization threshold energy density of silicon films was 0.53 J/cm^2 at 135 V for 3 μs-pulsed voltage and 0.60 J/cm^2 at 115 V for 5 μs-pulsed voltage application. The threshold energy densities were larger than that of 30-ns-pulsed laser crystallization at 0.16 J/cm^2.[15] Heat diffuses into deeper regions during micro-second heating than in the pulsed laser crystallization case, so that a higher heating energy is necessary for crystallization. Figure 4 shows a photograph of the bright field image of the transmission electron microscope (TEM) plane view for silicon films crystallized at 0.74 J/cm^2 for 5-μs-joule heating. The silicon region underlying the chromium strips was completely crystallized. Fine crystalline grains were formed with an average size of 100 nm. Our previous study of heat flow simulation and transient conductance measurement revealed that silicon films were heated to above the melting point.[9] Crystallization of silicon films occurred through melt followed by

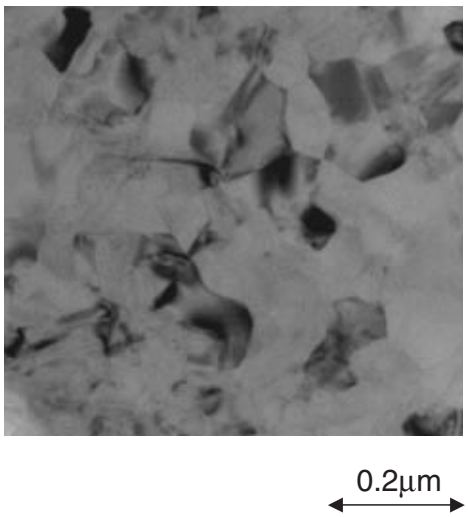

Fig. 4. Photograph of the bright field image of transmission electron microscope (TEM) plane view for silicon films crystallized at 0.74 J/cm^2 for 5-μs-joule heating.

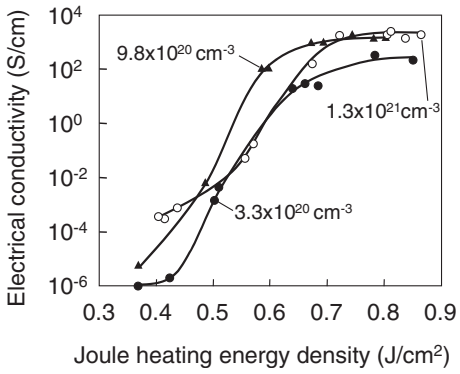

Fig. 5. Electrical conductivity as a function of the joule heating energy density for 5 μs-heating for silicon films with 3.3×10^{20} cm^{-3}–1.3×10^{21}-cm^{-3} phosphorous concentration.

solidification.

Figure 5 shows the electrical conductivity as a function of the joule heating energy density for 5 μs-heating for silicon films with 3.3×10^{20}–1.3×10^{21}-cm^{-3} phosphorous concentration. The electrical conductivity markedly increased as the joule heating energy density increased for every sample because doped silicon films were crystallized and dopant-phosphorus atoms were activated. The maximum conductivity increased from 250 S/cm to 2050 S/cm as the phosphorous concentration increased from 3.3×10^{20} cm^{-3} to 1.3×10^{21} cm^{-3}. Hall effect current measurements gave a carrier mobility of 13 cm^2/Vs and a carrier density of 1.0×10^{21} cm^{-3} for 1.3×10^{21} cm^{-3} phosphorus doping annealed at 0.7 J/cm^2. The high activation ratio and the high mobility were achieved by the rapid joule heating method.

Figure 6 shows the transfer characteristic of the n-channel and p-channel poly-Si TFTs with a channel length of 25 μm and a channel width of 70 μm fabricated at 5 μs joule heating energy densities at 0.75 and 0.74 J/cm^2, respectively. A sharp increase in the drain current with low gate voltage application was observed for the both TFTs. Figure 7 shows the effective carrier mobility and the threshold voltage obtained by a linear relationship of the drain current with the gate voltage. For n-channel TFTs, the carrier mobility increased from 115 to 570 cm^2/Vs as the joule heating

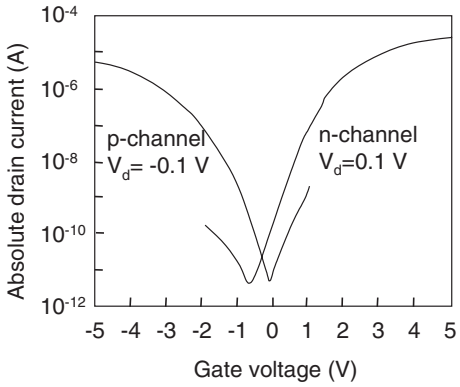

Fig. 6. Transfer characteristics of n-channel and p-channel poly-Si TFTs with a channel length of 25 μm and a channel width of 70 μm fabricated at joule heating energy densities at 0.75 and 0.74 J/cm^2, respectively.

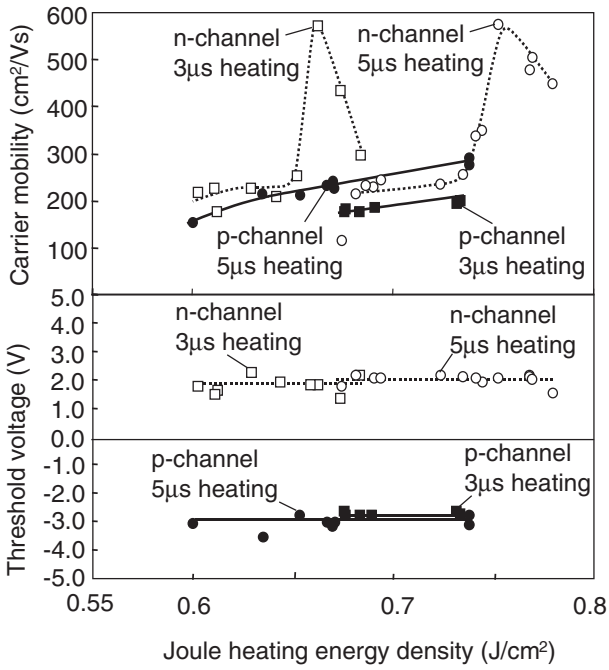

Fig. 7. The effective carrier mobility and the threshold voltage as functions of the joule heating energy density for n-channel and p-channel TFTs.

energy density increased from 0.67 to 0.75 J/cm^2 for the 5-μs-joule heating. The high carrier mobility probably resulted from a high crystalline volume ratio achieved by joule heating energy densities higher than the crystallization threshold. The effective carrier mobility increased from 210 to 570 cm^2/Vs as the joule heating energy density increased from 0.62 to 0.66 J/cm^2 for the 3-μs-joule heating. The 3-μs-joule heating resulted in crystallization at a low joule heating energy density because of high joule heating intensity caused by a high applied voltage. On the other hand, the effective mobility decreased above 0.75 J/cm^2 for the 5-μs-joule heating and above 0.66 J/cm^2 for the 3-μs-joule heating, as shown in Fig. 7. This probably resulted from a decrease in the crystalline volume ratio caused by micro-crystallization due to complete-melting followed by solidification.[16] For p-channel TFTs, the carrier mobility increased from 147 to 270 cm^2/Vs as the 5-μs-joule heating energy increased from 0.60 to 0.74 J/cm^2. The carrier mobility for the 5-μs-joule heating case was slightly higher than that for the 3-μs-joule heating case in the range from 0.67 to 0.74 J/cm^2, as shown in Fig. 7. The threshold voltage of n-channel TFTs was distributed between 1.8 and 2.2 V in the both cases of 3-μs and 5-μs-joule heating. It was distributed between −3.3 and −2.7 V for p-channel TFTs in both cases of 3-μs and 5-μs-joule heating, as shown in Fig. 7.

The threshold voltage was analyzed to estimate the density of defect states in polycrystalline silicon films using a numerical calculation program with the finite-element method combined with statistical thermodynamical conditions with localized defect states in silicon films.[17,18] The flat band voltage was estimated to be −0.5 V because of the difference of work function between aluminum and silicon. This allows us to interpret that defects trapping carriers are distributed symmetrically in the band gap, and that they increased the threshold voltage by 2.3–2.7 V for both

n-channel and p-channel TFTs. The numerical analysis indicated that the threshold voltage, 2.3–2.7 V, was governed by the density of defect states ranging from $9.8 \times 10^{11}\,cm^{-2}$ to $1.4 \times 10^{12}\,cm^{-2}$ in silicon films when Gaussian-type defect states with a width of 0.1 eV concentrated at the mid gap.

The experimental results in this study demonstrate that the present joule heating method results in the formation of polycrystalline silicon films and activation of dopant atoms, and that the present method is useful for fabricating poly-Si TFTs with a high mobility and a low threshold voltage. The joule heating method has an advantage of a simple heating system. An electrical voltage of about 100–150 volts with a pulse width of the order of micro seconds is easily generated from a simple electrical circuit. However, the present joule heating method requiress metal strips and intermediate insulating layers. Conventional semiconductor process technologies of lithography, etching and sputtering are useful for the formation of those layered structures consisting of metal and insulator.

4. Summary

The rapid heating properties of joule heating induced by electrical current flowing in chromium strips were applied in order to crystallize 50-nm-thick silicon films. The silicon films were crystallized by rapid joule heating above $0.53\,J/cm^2$ for 3-μs heating and above $0.6\,J/cm^2$ for 5-μs heating via 300-nm-thick SiO_2 intermediate layers. The average grain size was about 100 nm in the case of 5-μs joule heating at $0.74\,J/cm^2$. Activation of dopant atoms was also characterized. A high electrical conductivity of 2050 S/cm was achieved for 1.3×10^{21}-cm^{-3}-phosphorus doped silicon films in the case of 5-μs joule heating at $0.74\,J/cm^2$. Al-gate n-channel and p-channel poly-Si TFTs were fabricated with crystallization of silicon films and dopant activation induced by the rapid joule heating method. Defect reduction treatment of 13.56 MHz-remote-type-oxygen plasma at 100 W, 130 Pa and 250°C for 30 min was applied to the crystallized silicon films. Heat treatment at 200°C with 1.3×10^6-Pa-H_2O vapor for 3 h was also applied after TFT fabrication in order to improve the electrical properties of SiO_x gate insulator. N-channel TFTs have a high carrier mobility of $570\,cm^2/Vs$ in the case of 5-μs joule heating at $0.75\,J/cm^2$. The threshold voltage was distributed between 1.8 and 2.2 V. P-channel TFTs have a high carrier mobility of $270\,cm^2/Vs$ in the case of 5-μs joule heating at $0.74\,J/cm^2$. The threshold voltage distributed between −3.3 and −2.7 V. The numerical analysis indicated that the defect states localized with a density of $9.8 \times 10^{11}\,cm^{-2}$–$1.4 \times 10^{12}\,cm^{-2}$ in silicon films.

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